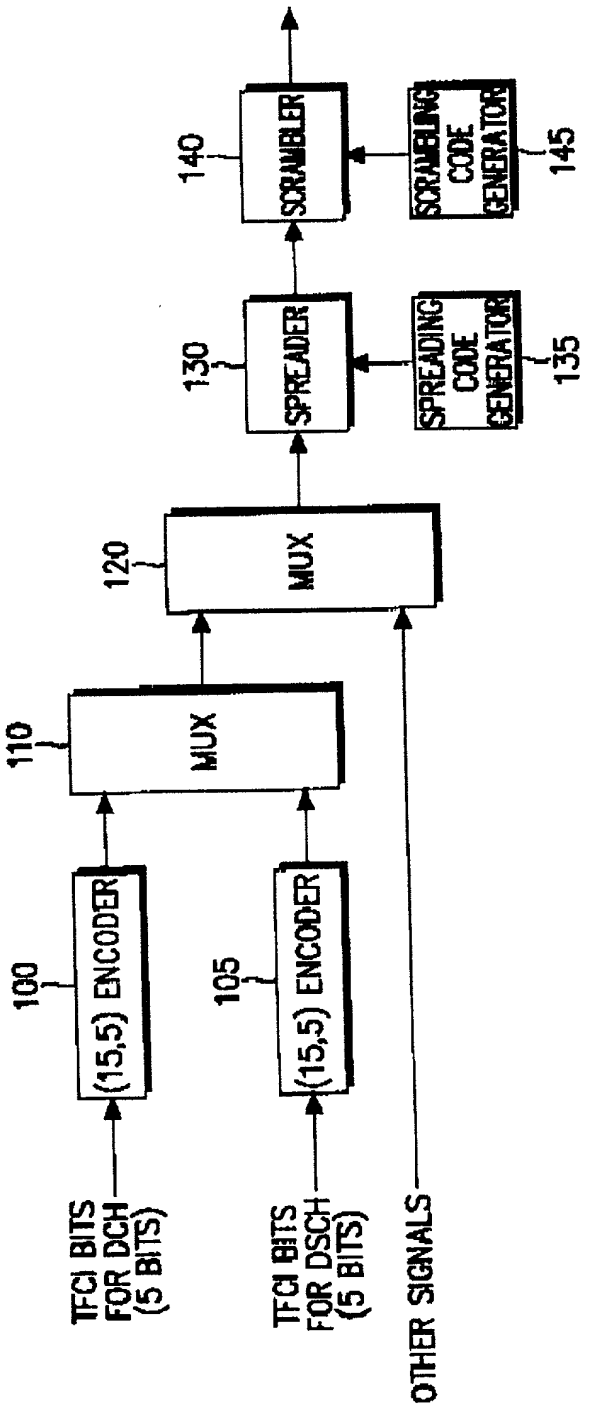

FIG. 1
(PRIOR ART)

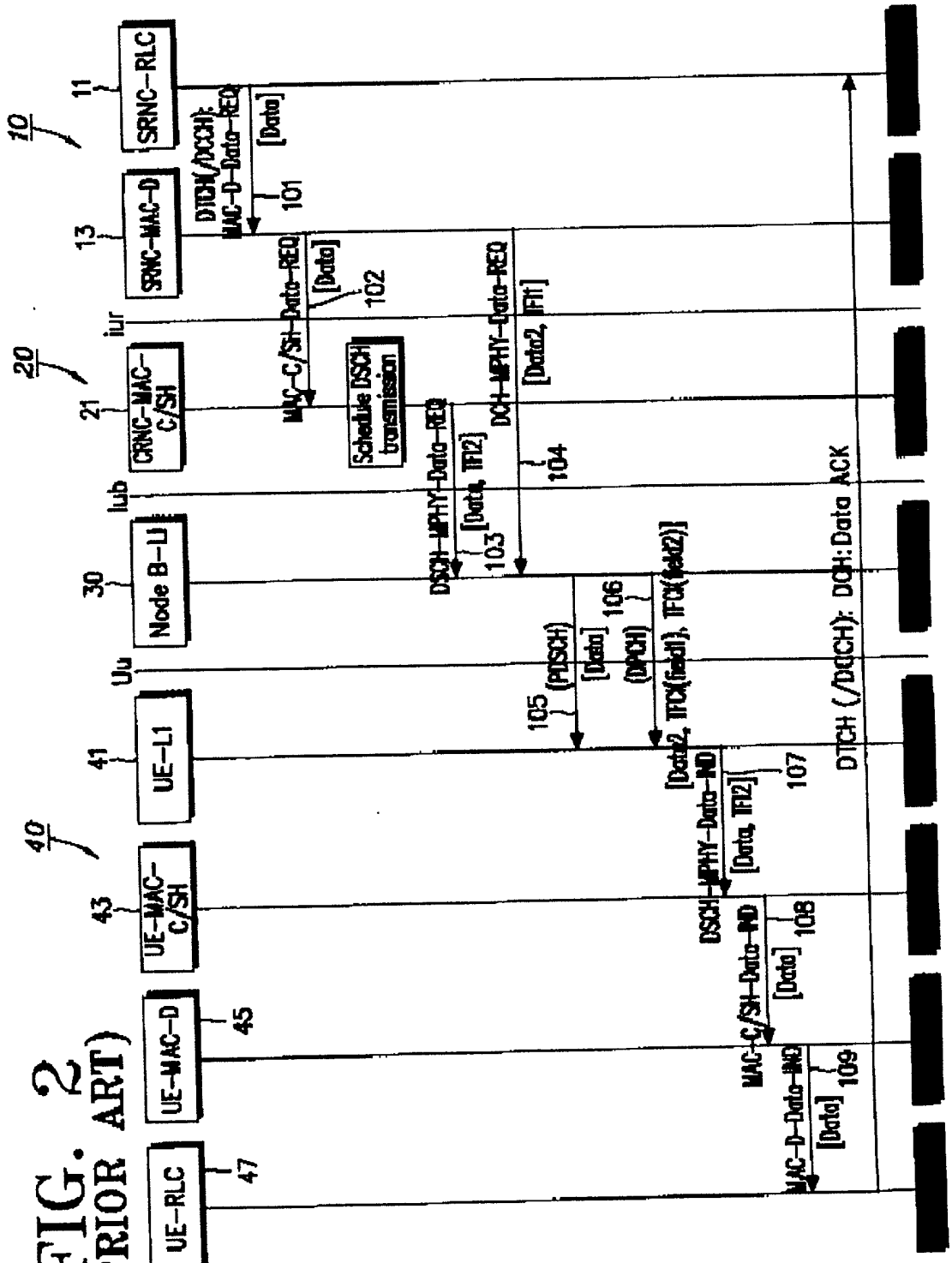

FIG. 2
(PRIOR ART)

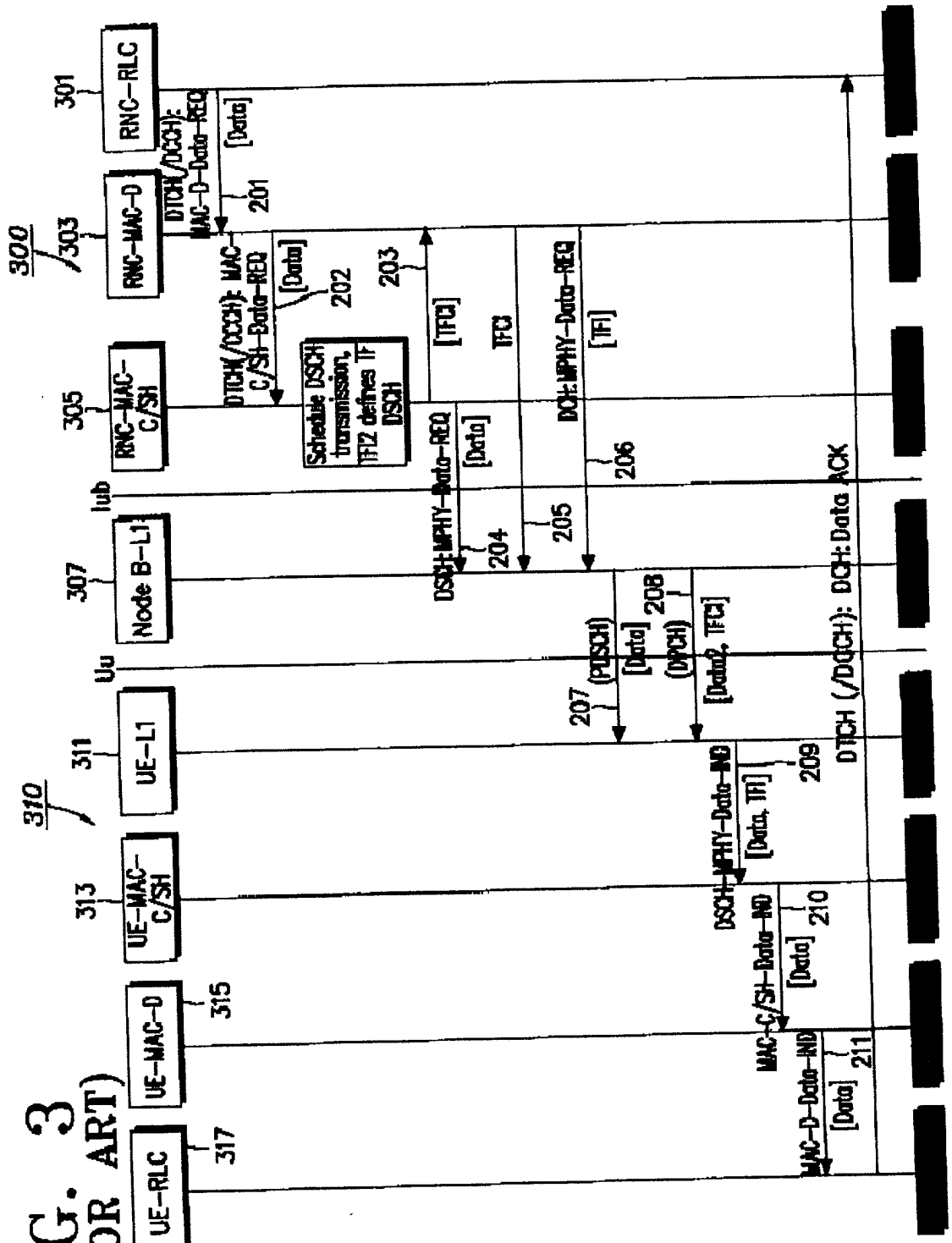

FIG. 3
(PRIOR ART)

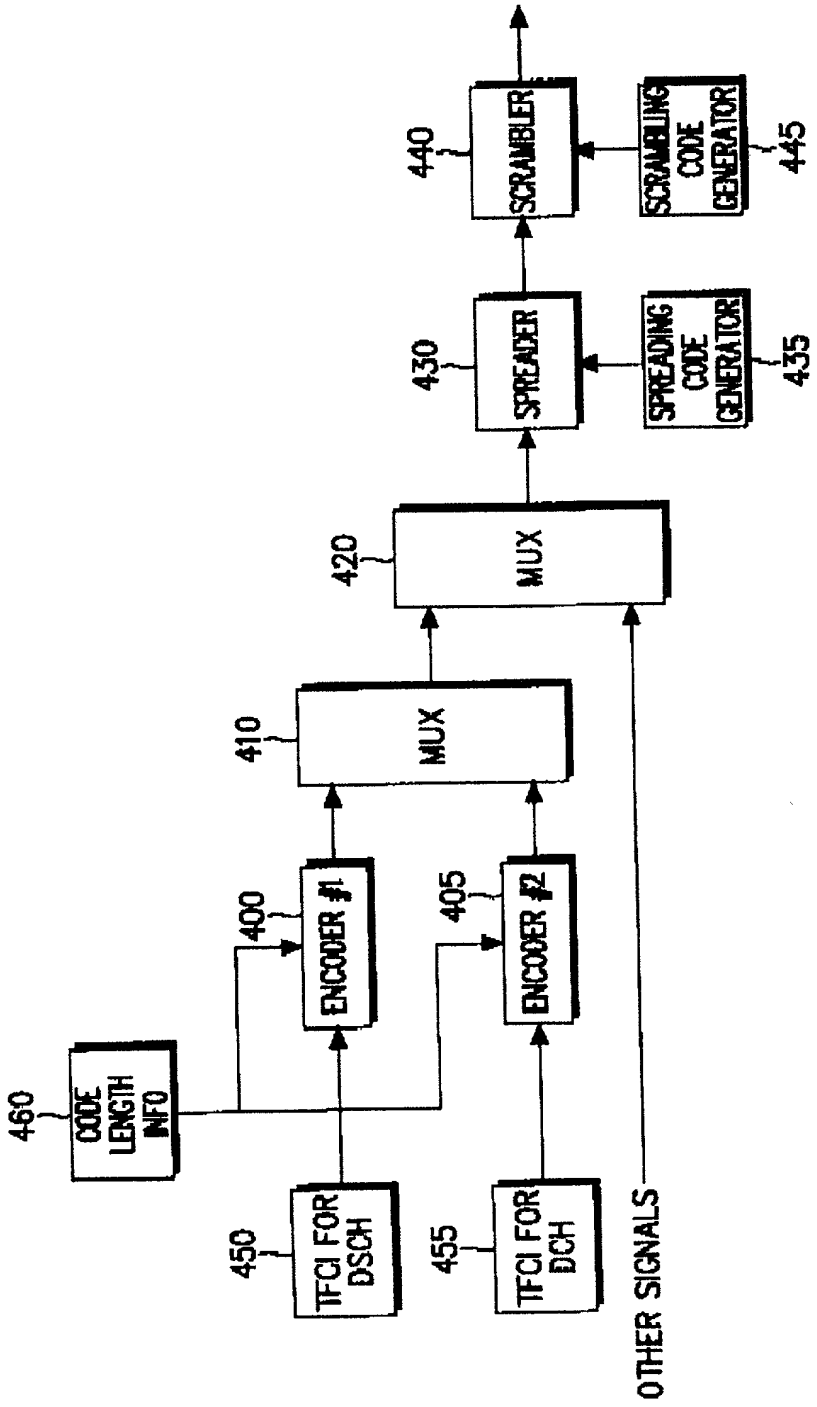
460
CODE LENGTH INFO
450
TFCI FOR DSCH
455
TFCI FOR DCH
OTHER SIGNALS
400
ENCODER #1
405
ENCODER #2
410
MUX
420
MUX
430
SPREADER
435
SPREADING CODE GENERATOR
440
SCRAMBLER
445
SCRAMBLING CODE GENERATOR

FIG. 4

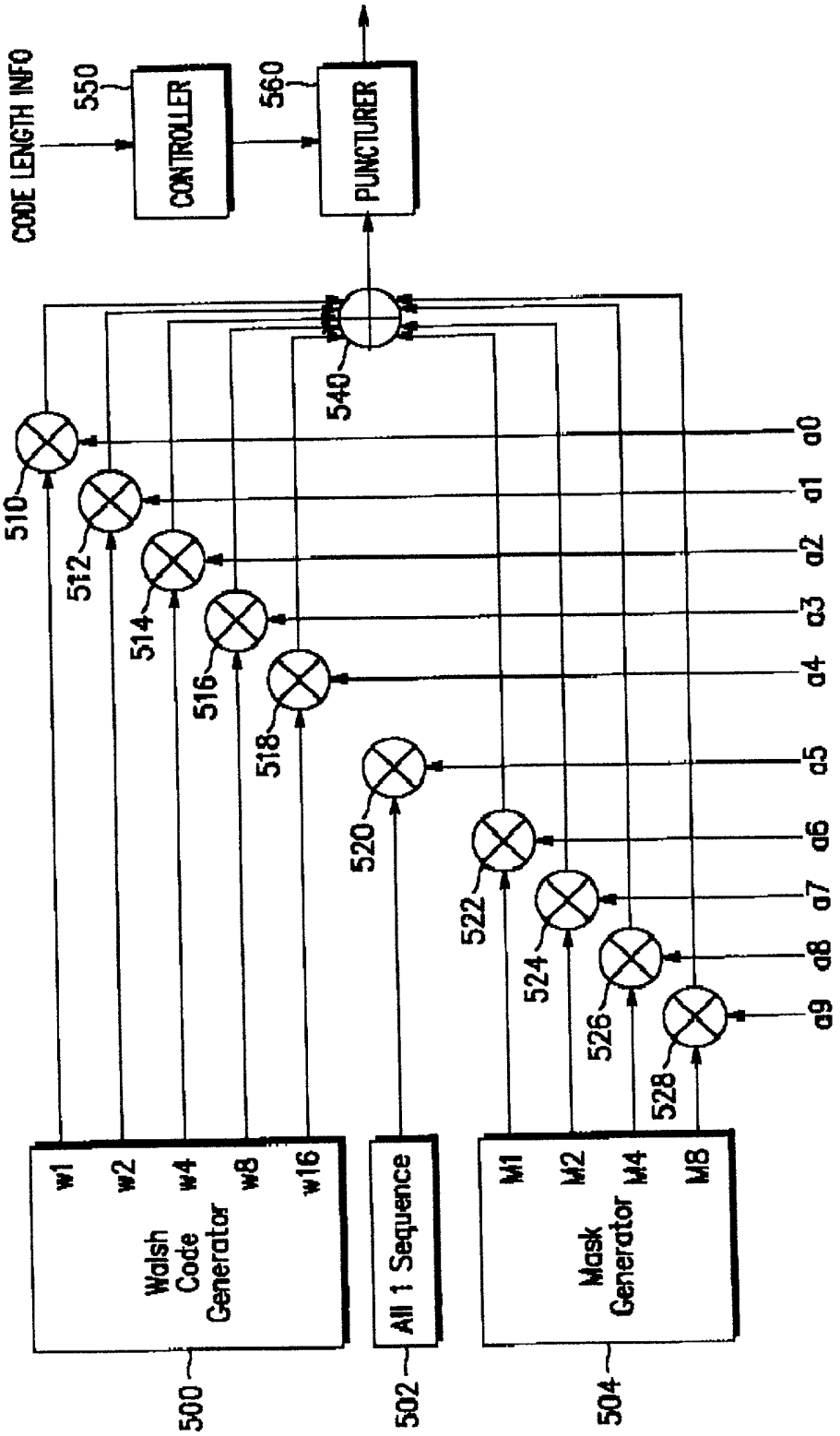
CODE LENGTH INFO
550
CONTROLLER
560
PUNCTURER
540
510
512
514
516
518
520
522
524
526
528
a0
a1
a2
a3
a4
a5
a6
a7
a8
a9
w1
w2
w4
w8
w16
Walsh Code Generator
500
All 1 Sequence
502
M1
M2
M4
M8
Mask Generator
504

FIG. 5

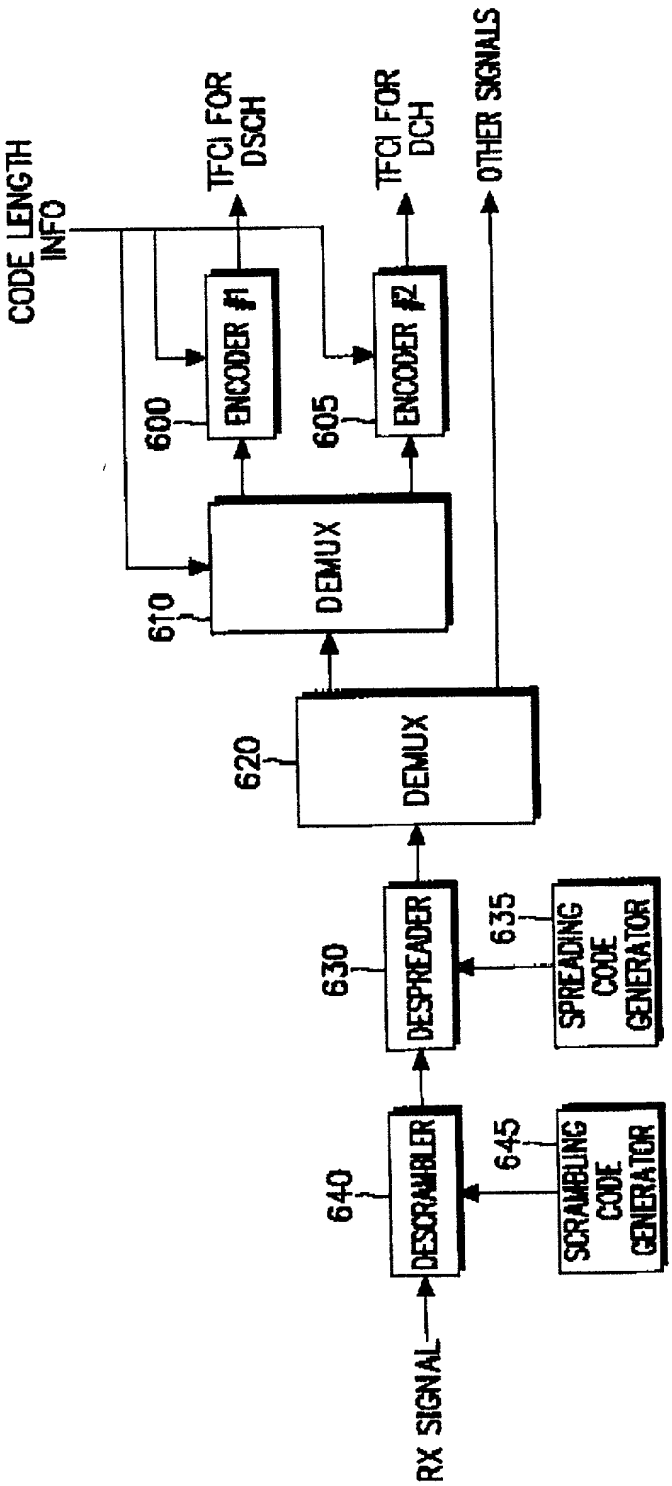
RX SIGNAL
640
DESCRAMBLER
645
SCRAMBLING CODE GENERATOR
630
DESPREADER
635
SPREADING CODE GENERATOR
620
DEMUX
610
DEMUX
600
ENCODER #1
605
ENCODER #2
CODE LENGTH INFO
TFCI FOR DSCH
TFCI FOR DCH
OTHER SIGNALS

FIG. 6

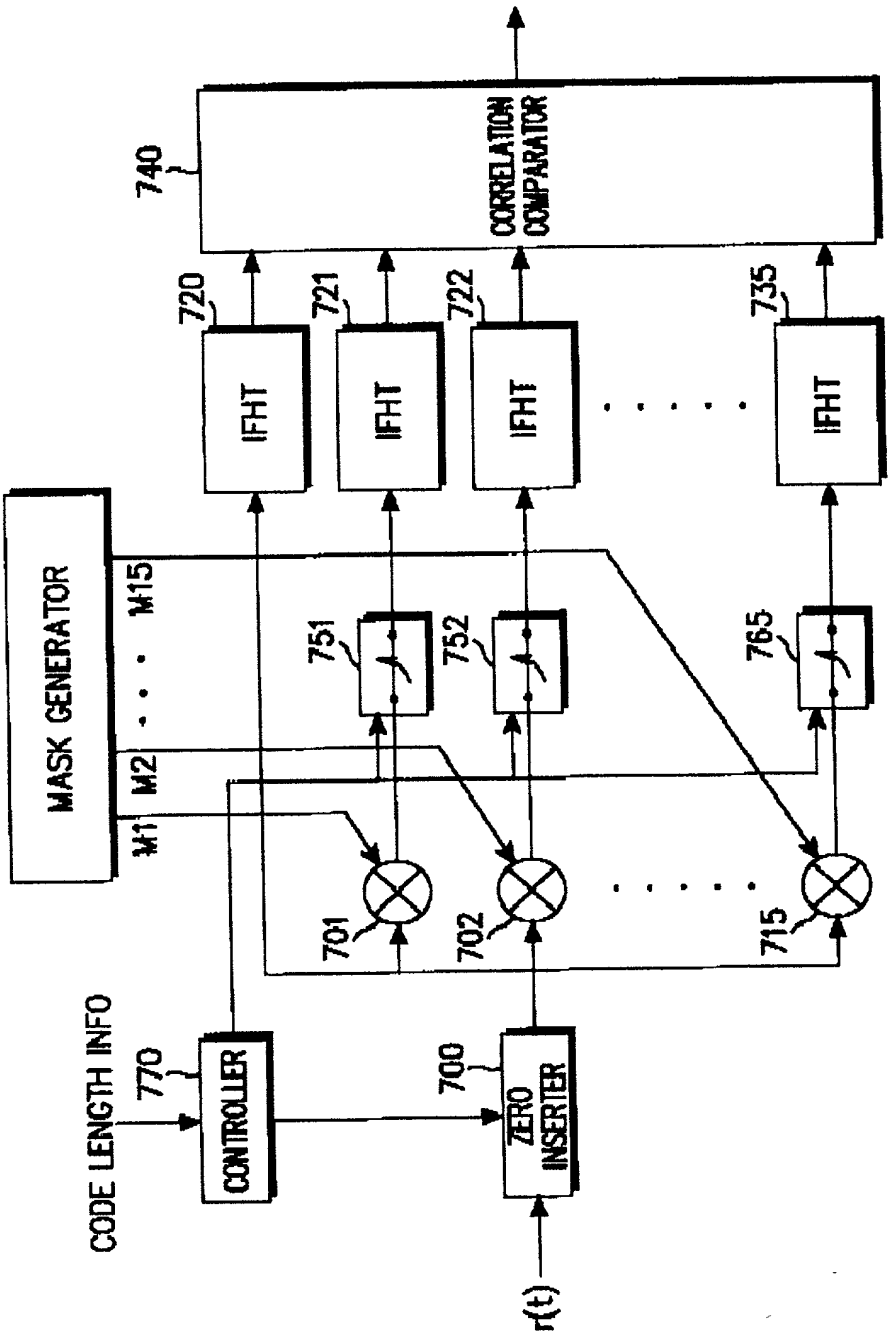
CORRELATION COMPARATOR
740
IFHT
720
721
722
735
MASK GENERATOR
M1
M2
M15
751
752
765
701
702
715
CODE LENGTH INFO
770
CONTROLLER
700
ZERO INSERTER
r(t)

FIG. 7

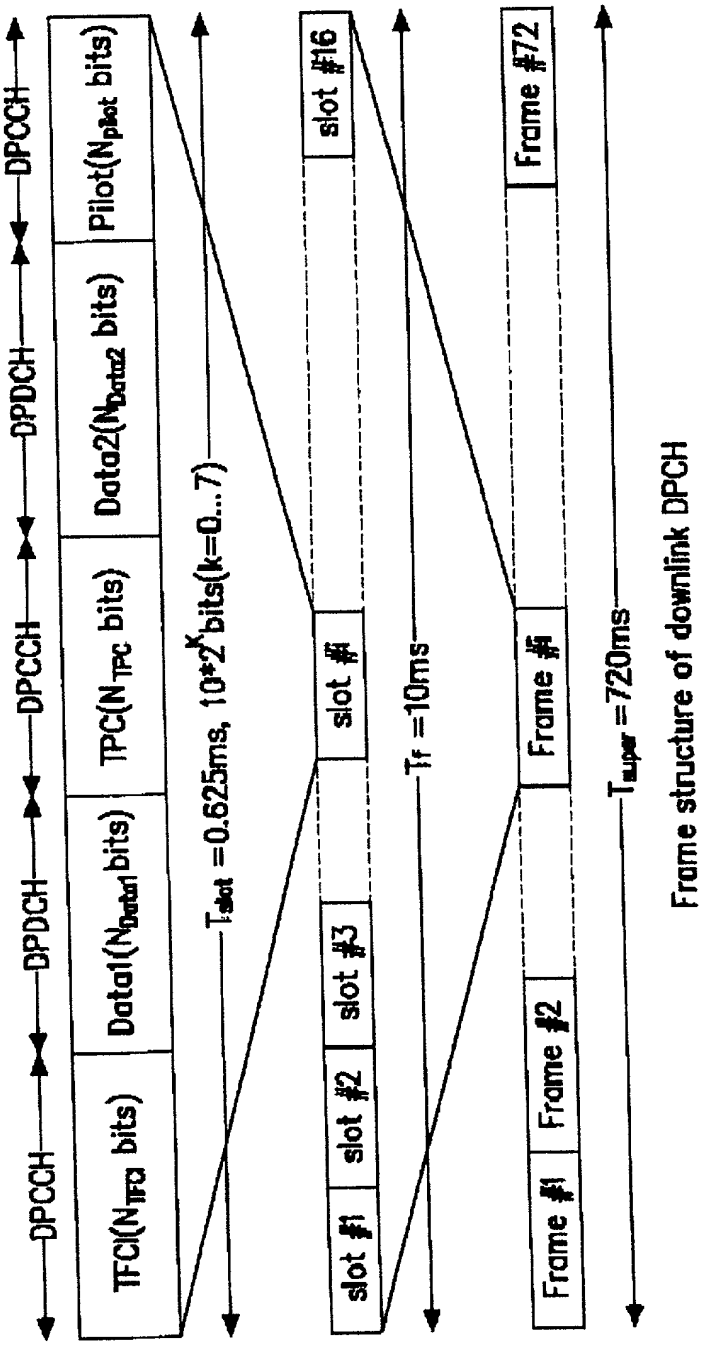
DPCCH
DPDCH
DPCCH
DPDCH
DPCCH
TFCI(N_{TFCI} bits)
Data1(N_{data1} bits)
TPC(N_{TPC} bits)
Data2(N_{data2} bits)
Pilot(N_{pilot} bits)
T_{slot} =0.625ms, 10*2^k bits(k=0...7)
slot #1
slot #2
slot #3
slot #4
slot #16
T_f =10ms
Frame #1
Frame #2
Frame #4
Frame #72
T_{super} =720ms
Frame structure of downlink DPCH

FIG. 8

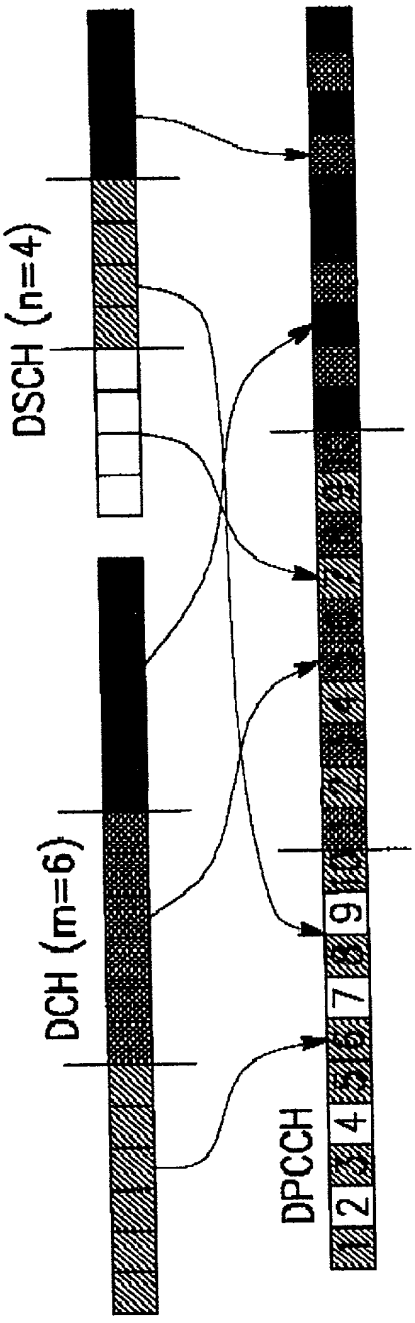

FIG. 9

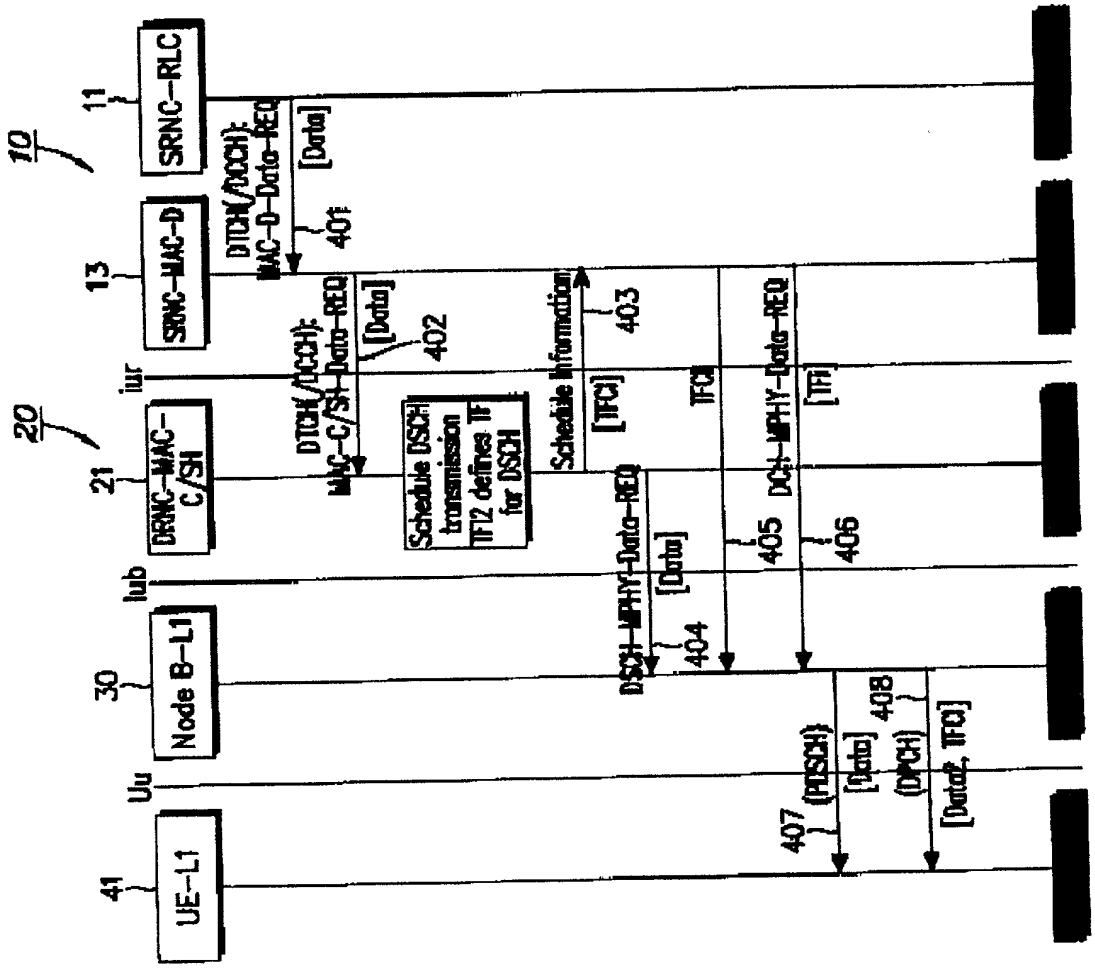
10
11
SRNC-RLC
13
SRNC-MAC-D
20
21
DRNC-MAC-C/SH
30
Node B-L1
41
UE-L1
Iur
Iub
Uu
DTCH/DCCH: MAC-D-Data-REQ
[Data]
401
DTCH/DCCH: MAC-C/SH-Data-REQ
[Data]
402
Schedule DSCH transmission TFI2 defines TF for DSCH
Schedule Information
[TFCI]
403
DSCH-MPHY-Data-REQ
[Data]
404
TFCI
DCH-MPHY-Data-REQ
[TFI]
405
406
407
(PRSCH)
[Data]
408
(DPCH)
[Data#, TFCI]

FIG. 10

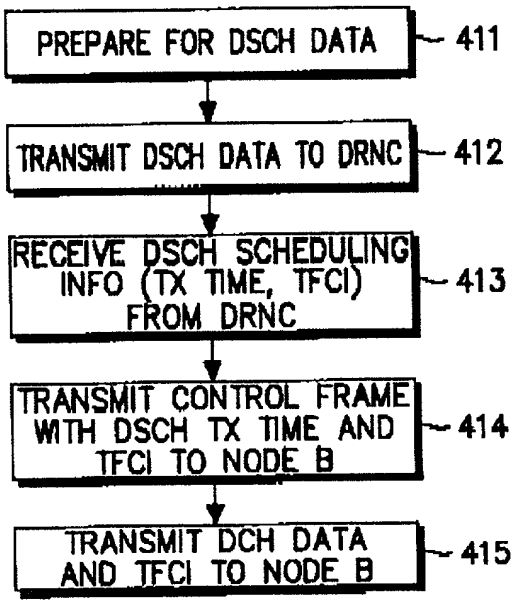
PREPARE FOR DSCH DATA
411
TRANSMIT DSCH DATA TO DRNC
412
RECEIVE DSCH SCHEDULING INFO (TX TIME, TFCI) FROM DRNC
413
TRANSMIT CONTROL FRAME WITH DSCH TX TIME AND TFCI TO NODE B
414
TRANSMIT DCH DATA AND TFCI TO NODE B
415

FIG. 11

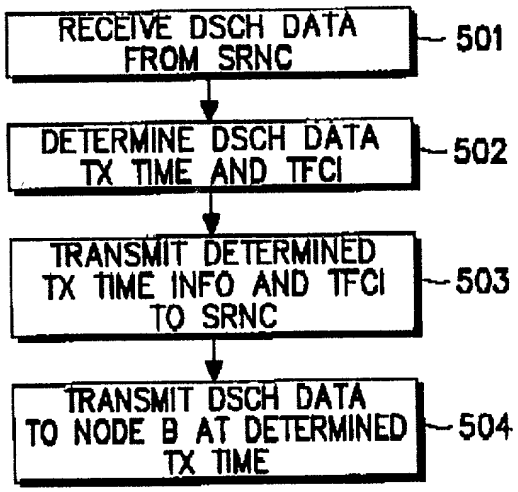

FIG. 12

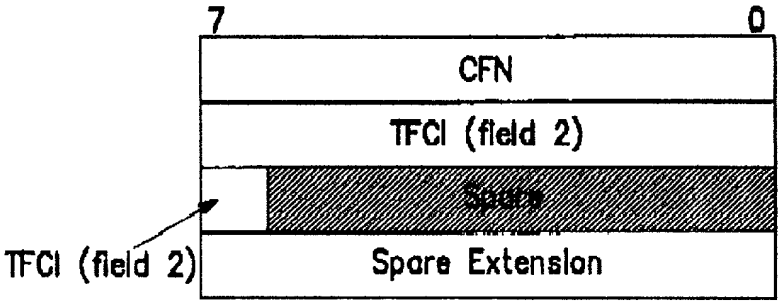

FIG. 13